three voltage level wordline, or control gate, scheme is used to eliminate errors in detection due to over erased cells. A guaranteed off-state voltage is used to guarantee that even over erased cells are in the off-state during a bit line check. A method to verify and correct under erased memory cells in a memory array is achieved. Cells are selectively re-erased if an under erase condition is detected. A method to detect and correct over erased memory cells in a memory array is achieved. Cells are selectively pulsed with a correction voltage if an over erase condition is detected.

As shown in the preferred embodiments, the novel method for erasing a Flash memory device provides an effective alternative to the prior art.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method to test ~~the~~ an erase condition of memory cells in a memory array device, said method comprising:

altering the erase condition of a section of said memory array device to form an erased section and non-erased sections;

forcing control gates of said memory cells in said non-erased sections to a normal off-state voltage sufficient to turn off erased cells;

forcing control gates of said memory cells in non-selected subsections of said erased section to a guaranteed off-state voltage that will turn off erased cells including those that are over erased;

forcing control gates of said memory cells in a selected subsection of said erased section to a check voltage;

thereafter measuring bitline current of said selected subsection of said erased section to determine erase condition of said selected subsection of said ~~erase~~ erased section.

2. The method according to Claim 1 wherein said erase condition comprises an under erase condition.

3. The method according to Claim 1 wherein said erase condition comprises an over erase condition.

4. The method according to Claim 1 wherein said memory array

device comprises memory cells selected from the group consisting of: OR array, NOR array, ETOX NOR array, and AND array.

5. The method according to Claim 1 further comprising pre-programming said memory array device prior to said step of altering the erase condition of a section of said memory array device.

6. The method according to Claim 1 further comprising correcting erase condition of said selected subsection of said erase section if said erase condition comprises one of the group consisting of: under erase condition and over erase condition.

7. The method according to Claim 1 wherein said normal off-state voltage comprises a value of about 0 Volts and wherein said guaranteed off-state voltage comprises a value of about -4 Volts.

8. A method to detect and correct an under erase condition in memory cells in a memory array device, said method comprising:

erasing a section of said memory array device to form an erased section and non-erased sections;

enabling subsequent erasing of all subsections of said erased section;

setting a starting memory address and thereby selecting a subsection of said erased section;

thereafter detecting under erased memory cells in said selected subsection of said erased section wherein said detecting comprises:

forcing control gates of said memory cells in said non-erased sections to a normal off-state voltage sufficient to turn off erased cells;

forcing control gates of said memory cells in non-selected subsections of said erased section to a guaranteed off-state voltage that will turn off erased cells including those that are over erased;

forcing control gates of said memory cells in a selected subsection of said erased section to an under erase check voltage;

thereafter measuring bitline current of said selected subsection of said erased section to determine said under erase condition of said selected subsection of said erase section and disabling subsequent erasing of said selected subsection of said erased section if said under erase condition does not exist;

thereafter incrementing to next said memory address

and thereby selecting a new selected subsection of said erased section; and

repeating said steps for said detecting under erased memory cells until every said subsection of said erased section is detected; and

thereafter, correcting said under erased cell by erasing said subsections of said erased section wherein said subsequent erasing remains enabled.

9. The method according to Claim 8 wherein said memory array device comprises memory cells selected from the group consisting of: OR array, NOR array, ETOX NOR array, and AND array.

10. The method according to Claim 8 further comprising pre-programming said memory array device prior to said step of erasing a section of said memory array device to form an erased section and non-erased sections.

11. The method according to Claim 8 wherein said normal off-state voltage comprises a value of about 0 Volts and wherein said guaranteed off-state voltage comprises a value of about -4 Volts.

12. The method according to Claim 8 further comprising

repeating steps of said method until erasing is disabled for every subsection of said erased section, said repeating steps comprising:

setting a starting memory address and thereby selecting a subsection of said erased section;

thereafter detecting under erased memory cells in said selected subsection of said erased section; and

thereafter, correcting said under erased cell by erasing said subsections of said erased section wherein said subsequent erasing remains enabled.

13. A method to detect and correct an over erase condition in memory cells in a memory array device, said method comprising:

erasing a section of said memory array device to form an erased section and non-erased sections;

setting a starting memory address and thereby selecting a subsection of said erased section; and

thereafter detecting and correcting over erased memory cells in said selected subsection of said erased section wherein said detecting and correcting comprises:

forcing control gates of said memory cells in said non-erased sections to a normal off-state voltage sufficient to turn off erased cells;

forcing control gates of said memory cells in non-selected subsections of said erased section to a

guaranteed off-state voltage that will turn off erased cells including those that are over erased;

forcing control gates of said memory cells in a selected subsection of said erased section to an over erased check voltage;

thereafter measuring bitline current of said selected subsection of said erased section to determine said over erase condition of said selected subsection of said erase section and pulsing a correction voltage on control gates of said memory cells of said selected subsection of said erased section if an over erase condition exists;

thereafter incrementing to next said memory address and thereby selecting a new selected subsection of said erased section; and

thereafter repeating said steps until every said subsection of said erased section is over erase detected and corrected.

14. The method according to Claim 13 wherein said memory array device comprises memory cells selected from the group consisting of: OR array, NOR array, ETOX NOR array, and AND array.

15. The method according to Claim 13 further comprising

pre-programming said memory array device prior to said step of erasing a section of said memory array device.

16. The method according to Claim 13 wherein said normal off-state voltage comprises a value of about 0 Volts and wherein said guaranteed off-state voltage comprises a value of about -4 Volts.

17. The method according to Claim 13 further comprising:

initializing a correction counter prior to said step of detecting and correcting over erased memory cells;

incrementing said correction counter for each occurrence of said pulsing a correction voltage on control gates; and

failing said selected subsection if said correction counter exceeds a maximum value.

18. The method according to Claim 13 wherein said pulsing a correction voltage comprises a correction voltage value given by:

$$V_{CORRECTION} = V_{INITIAL} + (V_{STEP} \text{ X } COUNTER_{CORRECTION}),$$

wherein said $V_{CORRECTION}$ is the peak value of said pulsing, wherein said $V_{INITIAL}$ is the peak value of said pulsing for the first pass, wherein said V_{STEP} is a voltage increment for each pass, and wherein said $COUNTER_{CORRECTION}$ is the value of said correction counter.

19. A method to erase memory cells in a memory array device, including detection and correction of under erase and detection and correction of over erase, said method comprising:

erasing a section of said memory array device to form an erased section and non-erased sections;

enabling subsequent erasing of all subsections of said erased section;

setting a starting memory address and thereby selecting a subsection of said erased section;

thereafter detecting under erased memory cells in said selected subsection of said erased section wherein said detecting comprises:

forcing control gates of said memory cells in said non-erased sections to a normal off-state voltage sufficient to turn off erased cells;

forcing control gates of said memory cells in non-selected subsections of said erased section to a guaranteed off-state voltage that will turn off erased cells including those that are over erased;

forcing control gates of said memory cells in a selected subsection of said erased section to an under erased check voltage;

thereafter measuring bitline current of said selected subsection of said erased section to determine said under

erase condition of said selected subsection of said erase section and disabling subsequent erasing of said selected subsection of said erased section if said under erase condition does not exist;

thereafter incrementing to next said memory address and thereby selecting a new selected subsection of said erased section; and

thereafter repeating said steps until every said subsection of said erased section is detected;

thereafter, correcting said under erased cell by erasing said subsections of said erased section wherein said subsequent erasing remains enabled;

thereafter setting a starting memory address and thereby selecting a subsection of said erased section; and

thereafter detecting and correcting over erased memory cells in said selected subsection of said erased section wherein said detecting and correcting comprises:

forcing control gates of said memory cells in said non-erased sections to a normal off-state voltage sufficient to turn off erased cells;

forcing control gates of said memory cells in non-selected subsections of said erased section to a guaranteed off-state voltage that will turn off erased cells including those that are over erased;

forcing control gates of said memory cells in a

selected subsection of said erased section to an over erased check voltage;

thereafter measuring bitline current of said selected subsection of said erased section to determine said over erase condition of said selected subsection of said erase section and pulsing a correction voltage on control gates of said memory cells of said selected subsection of said erased section if an over erase condition exists;

thereafter incrementing to next said memory address and thereby selecting a new selected subsection of said erased section; and

thereafter repeating said steps until every said subsection of said erased section is detected and corrected.

20. The method according to Claim 19 wherein said memory array device comprises memory cells selected from the group consisting of: OR array, NOR array, ETOX NOR array, and AND array.

21. The method according to Claim 19 further comprising pre-programming said memory array device prior to said step of erasing a section of said device to form an erased section and non-erased sections.

22. The method according to Claim 19 wherein said normal off-state voltage comprises a value of about 0 Volts and wherein said guaranteed off-state voltage comprises a value of about -4 Volts.

23. The method according to Claim 19 further comprising repeating steps of said method until erasing is disabled for every subsection of said erased section, said repeating steps comprising:

setting a starting memory address and thereby selecting a subsection of said erased section;

thereafter detecting under erased memory cells in said selected subsection of said erased section; and

thereafter, correcting said under erased cell by erasing said subsections of said erased section wherein said subsequent erasing remains enabled.

24. The method according to Claim 19 further comprising:

initializing a correction counter prior to said step of detecting and correcting over erased memory cells;

incrementing said correction counter for each occurrence of said pulsing a correction voltage on control gates; and

failing said selected subsection if said correction counter exceeds a maximum value.

25. The method according to Claim 19 wherein said pulsing a correction voltage comprises a correction voltage value given by:

$$V_{CORRECTION} = V_{INITIAL} + (V_{STEP} \text{ X } COUNTER_{CORRECTION}),$$

wherein said $V_{CORRECTION}$ is the peak value of said pulsing, wherein said $V_{INITIAL}$ is the peak value of said pulsing for the first pass, wherein said V_{STEP} is a voltage increment for each pass, and wherein said $COUNTER_{CORRECTION}$ is the value of said correction counter.